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A Fully Synthesizable Digital Low Dropout Regulator(LDO) with Fast Transient Response

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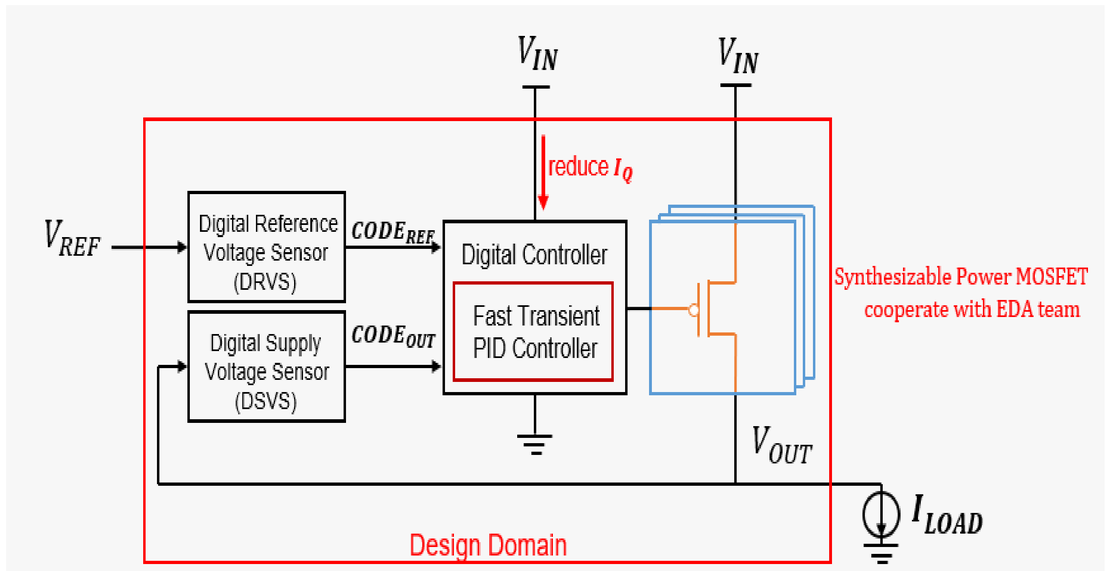
Introduction

- Low Dropout Regulator(LDO)
  - The purpose of LDO is to provide stable supply voltage for the back-end circuits.
- Comparisons of digital and analog LDOs

	Digital LDO	Analog LDO
Dropout Voltage	**Low**	Medium to High
Benefits from Technology Scaling	**More**	Fewer
Settling Time	**Fast**	Slow
Output Ripple	Large	**Small**
Quantization Error	Yes	No

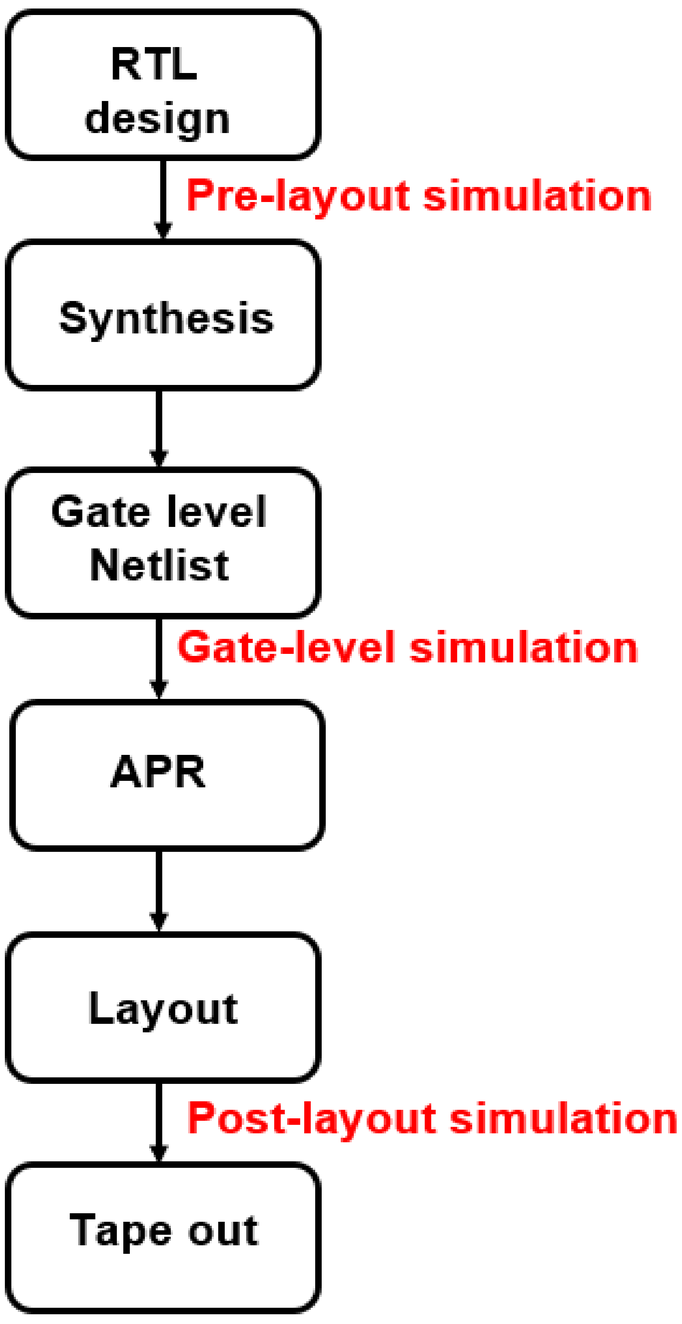
- Internet of thing(IoT) needs low supply and small area, digital LDO is a suitable choice.
- When the load current changes , digital LDO has faster transient response.

System Architecture



- The Digital Reference Voltage Sensor and Digital Supply Voltage Sensor will transfer voltage to digital code.
- The Digital Controller will turn on/off the power MOSFET according to the comparison result of $CODE_{OUT}$ and $CODE_{REF}$.
- We will cooperate with EDA team to make the power MOSFET synthesizable.

Design flow



- The whole digital LDO is synthesizable.
- The design flow will be similar with digital circuit design.
- APR stands for automatic placement and routing.

Specification

- The target of this work and the achievement of other works.

	This work	[1] ISSCC 2020	[2] VLSI 2019
V_{IN}	0.9V	0.7 to 1.05 V	0.5 to 1V
V_{OUT}	0.45 to 0.7V	0.65 to 0.95V	0.45 to 0.9V
Peak current efficiency @I_L	> 99% @1A	98.6% @3A	99.9% @0.1A
Current efficiency @I_L (light load current)	> 90% @0.1A	74% @0.1A	95% @1mA
V_{DROOP} @ΔI_L	< 150mV @1A	200mV @1.17A	94.1mV @124mA
I_Q	< 15mA	43mA	0.68mA
Fully Synthesis	yes	yes	no
FoM	< 2ps	5.2ps	4.3ps

$$FoM = I_Q \times \left(\frac{C_{out} \times V_{DROOP}}{\Delta I_L{}^2} + \frac{0.5}{SR}\right), \text{where SR} = \frac{\Delta I_L}{\Delta t}$$

- Optimizing the performance of transient response is the target of this work.
- Another target is to reduce the quiescent current of the digital controller, making current efficiency better.

References

- [1] Suyoung Bang, Wootaek Lim, Charles Augustine, Andres Malavasi, Muhammad Khellah, James Tschanz, Vivek De, "A Fully Synthesizable Distributed and Scalable All-Digital LDO in 10nm CMOS, " IEEE ISSCC, February 2020
- [2] S. J. Kim et al., "A 0.5-1V Input Event-Driven Multiple Digital Low-Dropout-Regulator System for Supporting a Large Digital Load," *IEEE Symp. VLSI Circuits*, pp. C128-C129, June 2019.